In the Claims:

Please Amend Claims 1, 4, 9, 13 and 24 as follows:

1. (currently amended) A device for electrostatic discharge input protection comprising:

a transistor with gate, source, drain and substrate terminals;

an input signal terminal coupled to said source terminal of said transistor;

a reference point coupled to said gate and substrate terminals of said transistor;

and

an ~~a~~ output signal terminal coupled to said drain terminal of said transistor;

where under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and the leakage current of said transistor is reduced to a sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and reduces its threshold voltage.

4. (currently amended) The device of claim 1 wherein said reference point comprises ~~Vss~~ the lower potential supply terminal Vss.

9. (currently amended) A low leakage Electrostatic Discharge (ESD) protection scheme comprising:

a plurality of low operating voltage devices, each device having at least one device input for receiving an input signal;

a plurality of input terminals for coupling an input signal to a device via a corresponding device input;

a plurality of transistors with gate, substrate, source and drain terminals,

each transistor providing an alternate pathway via a source terminal for signals from said plurality of input terminals; and

a reference coupled to corresponding gate and substrate terminals of said plurality of input protection transistors; and

a source voltage driving both said source terminals of said input protection transistors and said inputs of said low operating voltage devices;

wherein under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and ESD protection is achieved by coupling the source terminals of said plurality of transistors to said plurality of input terminals thereby limiting the leakage current of each of said transistors to a sub-threshold level even as said source voltage increases.

13. (currently amended) The protection scheme of claim 9 wherein said reference point comprises ~~Vss~~ the lower potential supply terminal Vss for said low voltage operating devices and said plurality of transistors.

24. (currently amended) The IC of claim 18 wherein said reference point is tied to said ~~Vss~~ lower potential supply terminal Vss.